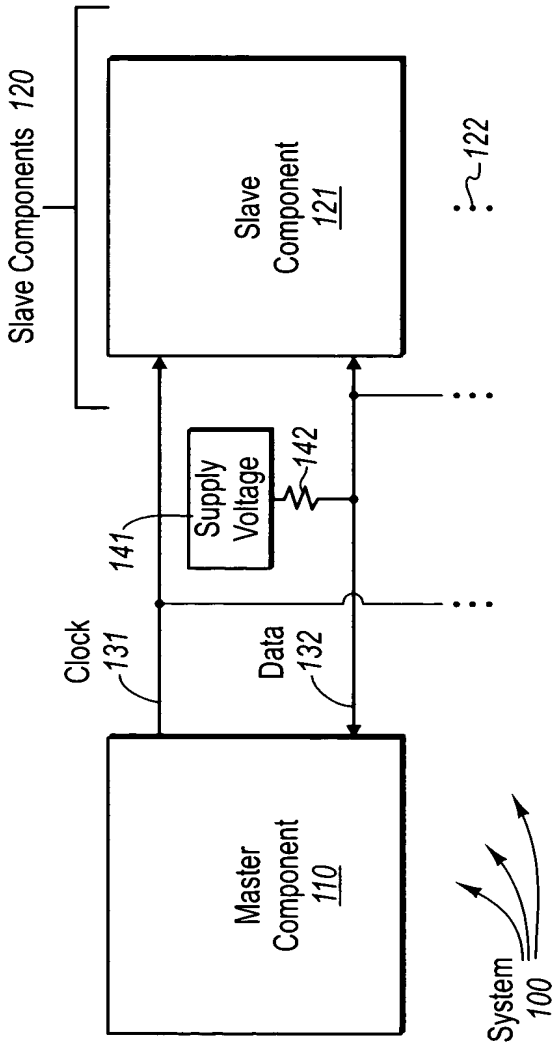
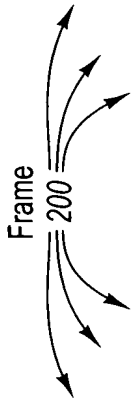


Fig. 1



Preamble 201	Frame Start 202	Operation 203	Device ID 204	ExtD 205	Basic Address 206	TA1 207	Bus Hold 208	Data 209	CRC 210	TA2 211	ACK 212	Error 213	Frame End 214

Fig. 2

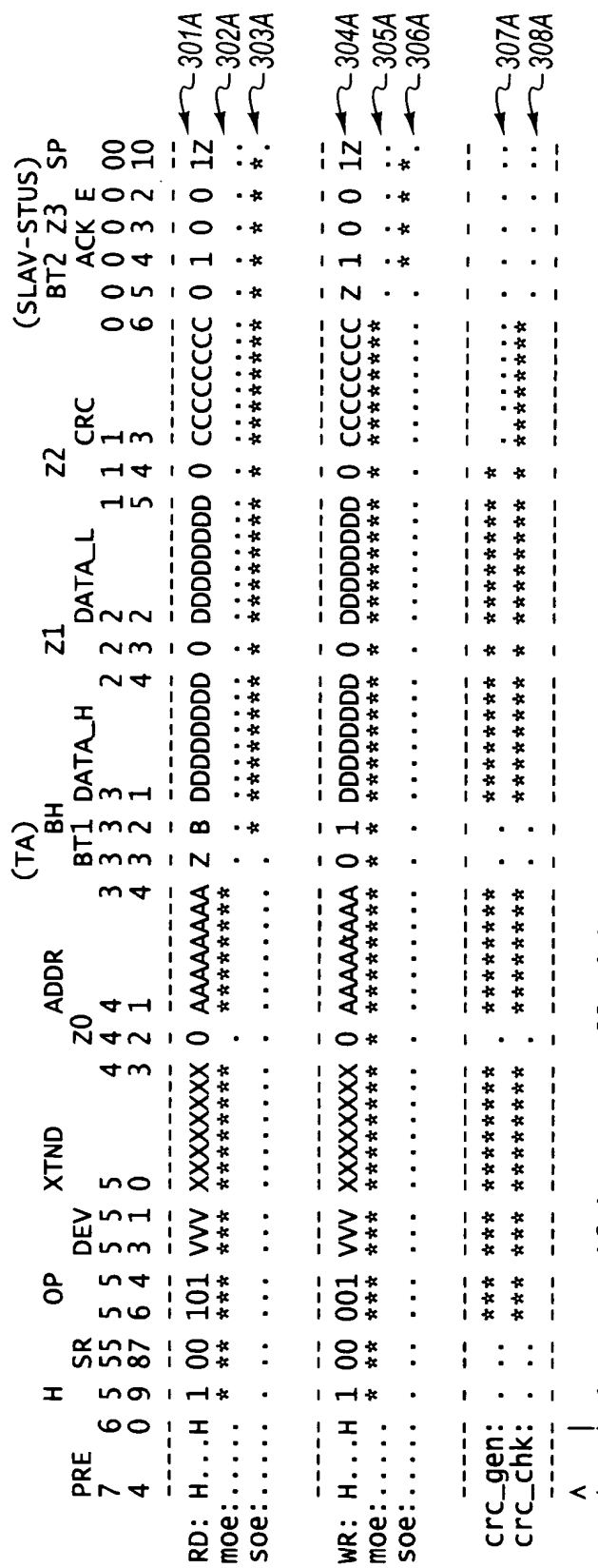

(TA)
(SLAV-STUS)
H
OP
XTND
ADDR
BH
Z1
Z2
BT2 Z3 SP
PRE
SR
DEV
Z0
BT1 DATA_H
DATA_L
CRC
ACK E
7 6 5 55 5 5 5 5 4 4 4 3 3 3 3 2 2 2 1 1 1 0 0 0 0 0 00
4 0 9 87 6 4 3 1 0 3 2 1 4 3 2 1 4 3 2 5 4 3 6 5 4 3 2 10
RD: H...H 1 00 101 VVV XXXXXXX 0 AAAAAAA Z B DDDDDDD 0 DDDDDDD 0 CCCCCCCC 0 1 0 0 0 1Z
moe:..... * ** *** ********* . ********* . ********* . ********* * ********* . . . . . .
soe:..... . .. . ********* * ********* * ********* . . * * * * . .
WR: H...H 1 00 001 VVV XXXXXXX 0 AAAAAAA 0 1 DDDDDDD 0 DDDDDDD 0 CCCCCCCC Z 1 0 0 1Z
moe:..... * ** *** ********* * ********* * * ********* * ********* * ********* . . . . . .
soe:..... . .. . ********* . ********* . ********* . ********* . * * * * . .
crc_gen: . .. *** ********* . ********* . ********* * ********* * ....
crc_chk: . .. *** ********* . ********* . ********* * ********* * ********* . . . . . .
(restart if input not all 1's)
301A
302A
303A
304A
305A
306A
307A
308A

Fig. 3A

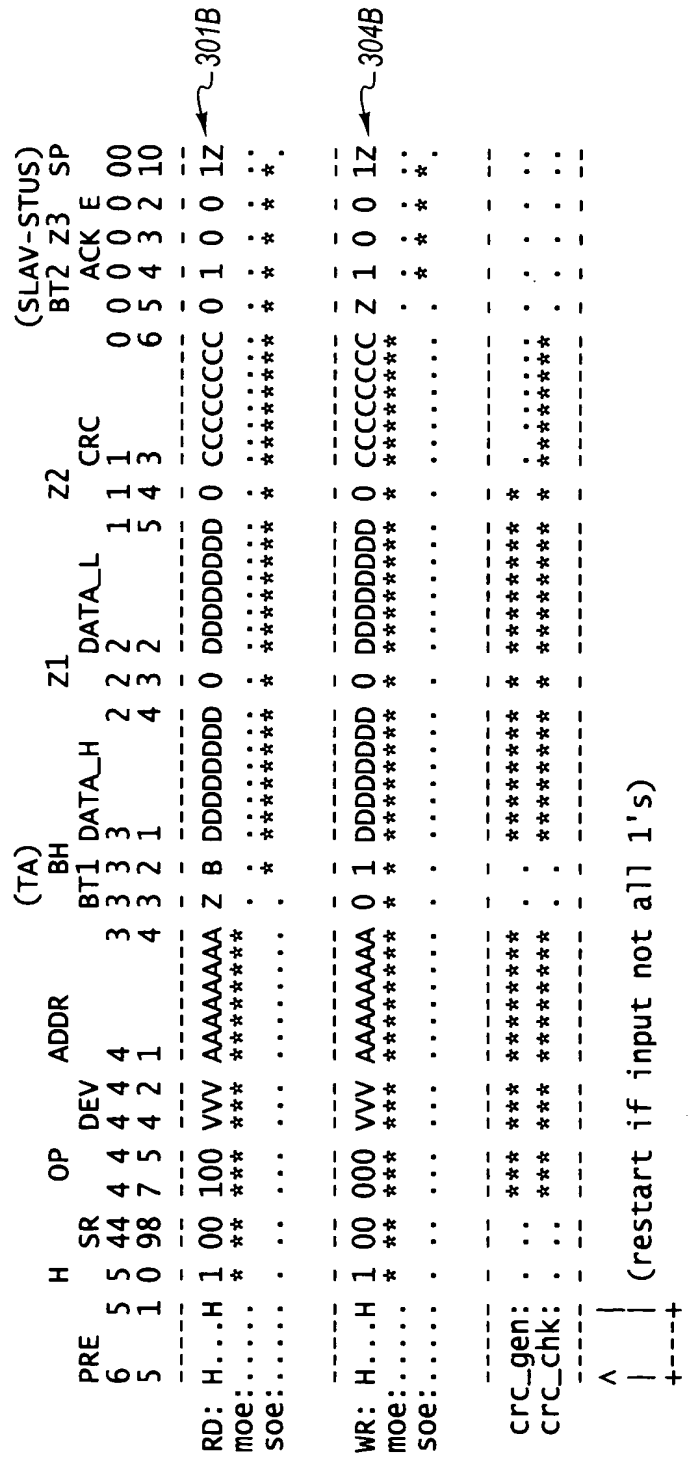

(TA)
(SLAV-STUS)
H
OP
ADDR
BH
Z1
Z2
BT2 Z3 SP
PRE
SR
DEV
BT1 DATA_H
DATA_L
CRC
ACK E
6 5 5 44 4 4 4 4 3 3 3 3 2 2 1 1 1 0 0 0 0 0 00
5 1 0 98 7 5 4 2 1 4 3 2 1 4 3 2 5 4 3 6 5 4 3 2 10
RD: H...H 1 00 100 VVV AAAAAAA Z B DDDDDDDD 0 DDDDDDDD 0 CCCCCCCC 0 1 0 0 1Z
301B
WR: H...H 1 00 000 VVV AAAAAAA 0 1 DDDDDDDD 0 DDDDDDDD 0 CCCCCCCC Z 1 0 0 1Z
304B
crc_gen:
crc_chk:
(restart if input not all 1's)

Fig. 3B

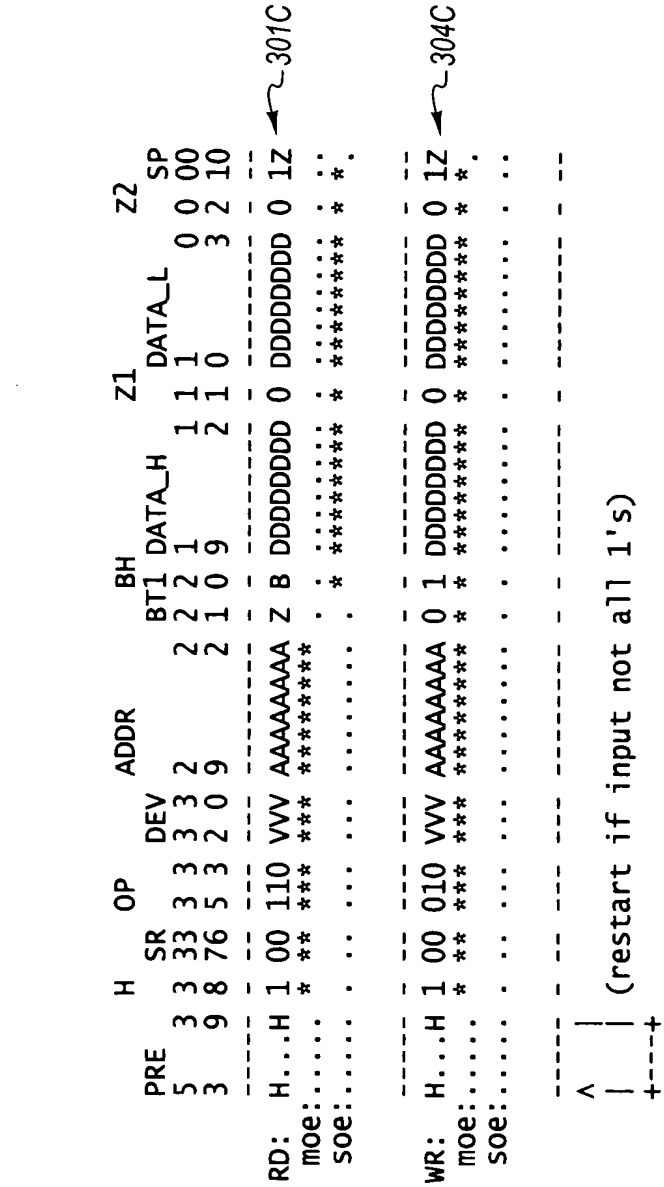

H OP ADDR BH Z1 Z2
PRE SR DEV BT1 DATA_H DATA_L SP
5 3 3 33 3 3 3 2 2 2 1 1 1 0 0 00
3 9 8 76 5 3 2 0 9 2 1 0 9 2 1 0 3 2 10
RD: H...H 1 00 110 VVV AAAAAAA Z B DDDDDDDD 0 DDDDDDD 0 1Z
moe:..... * ** *** *** ******** . . ..
soe:..... . .. . * ********* * ******** * *.
WR: H...H 1 00 010 VVV AAAAAAA 0 1 DDDDDDDD 0 DDDDDDD 0 1Z
moe:..... * ** *** *** ******** * * ********* * ******** * *.
soe:..... . .. .
(restart if input not all 1's)
301C
304C

Fig. 3C

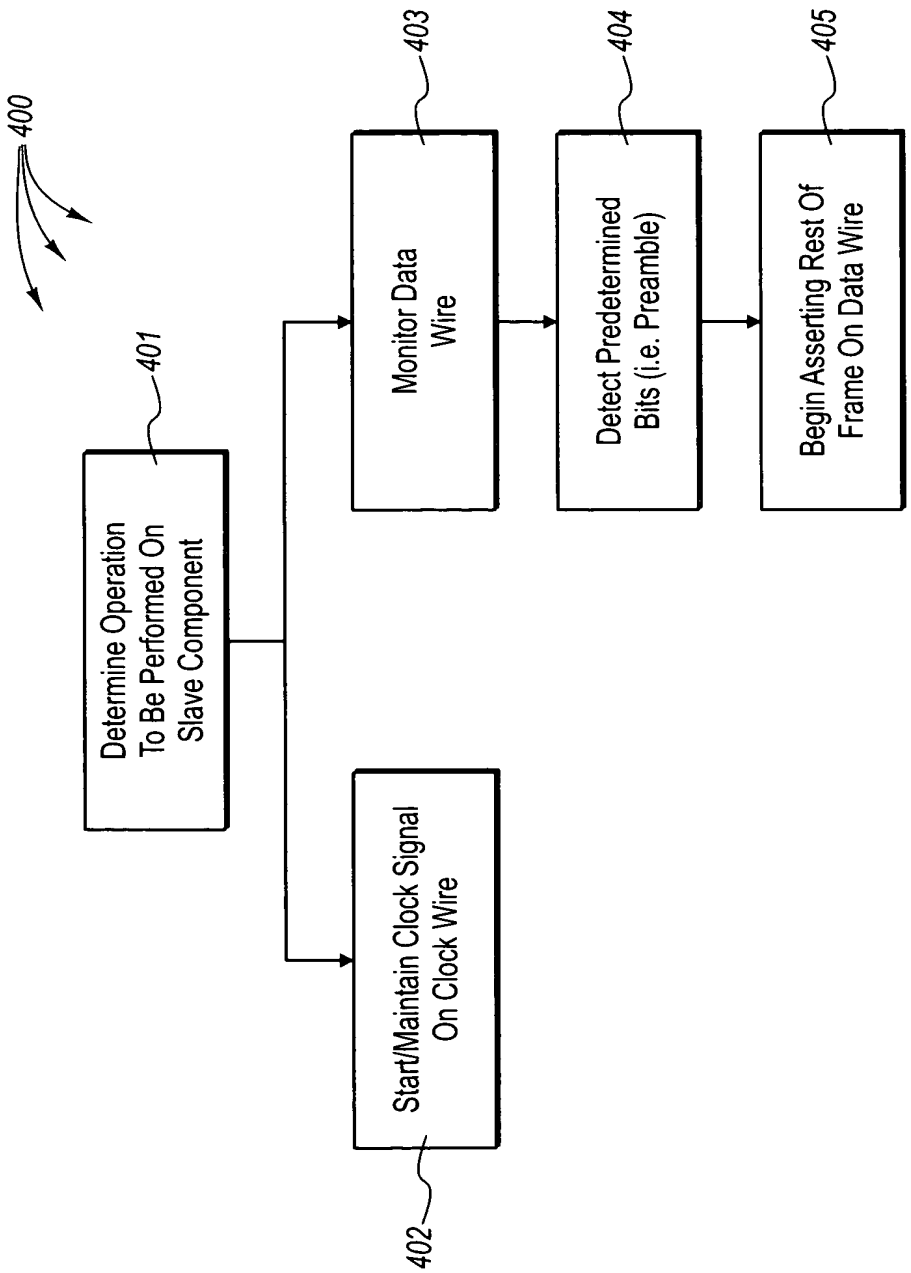

400
401
Determine Operation To Be Performed On Slave Component
402
Start/Maintain Clock Signal On Clock Wire
403
Monitor Data Wire
404
Detect Predetermined Bits (i.e. Preamble)
405
Begin Asserting Rest Of Frame On Data Wire

Fig. 4

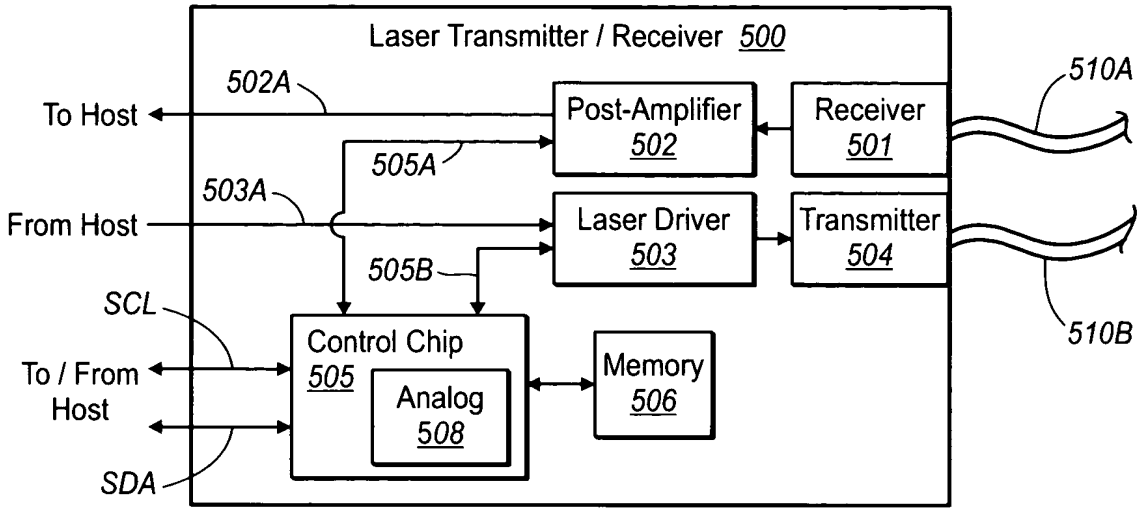

Laser Transmitter / Receiver 500
502A
To Host
Post-Amplifier 502
Receiver 501
510A
505A
503A
From Host
Laser Driver 503
Transmitter 504
505B
510B
SCL
Control Chip 505
Analog 508
Memory 506
To / From Host
SDA

Fig. 5

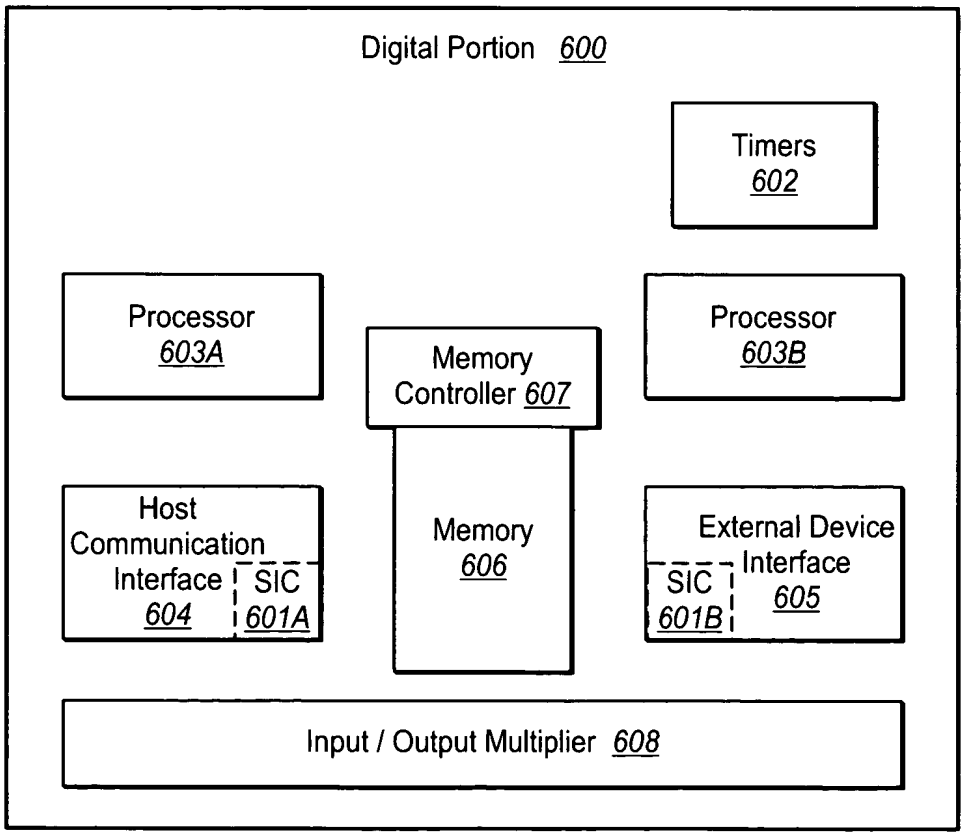

Digital Portion 600
Timers 602
Processor 603A
Memory Controller 607
Processor 603B
Host Communication Interface 604
SIC 601A
Memory 606
External Device Interface 605
SIC 601B
Input / Output Multiplier 608

Fig. 6

```
-------------------------------------------------------------
          PRE   ST OP PRT   DEV   TA ADDRESS/DATA     IDLE
          6   3 33 32 2   2 2   1 11 1              0 0
          4   3 21 09 8   4 3   9 87 6              1 0
--------- ----- -- -- ----- ----- -- ---------------- -
Address   1...1 00 00 PPPPP EEEEE 10 AAAAAAAAAAAAAAAA Z
Write     1...1 00 01 PPPPP EEEEE 10 DDDDDDDDDDDDDDDD Z
Read      1...1 00 11 PPPPP EEEEE Z0 DDDDDDDDDDDDDDDD Z
Read inc. 1...1 00 10 PPPPP EEEEE Z0 DDDDDDDDDDDDDDDD Z
--------- ----- -- -- ----- ----- -- ---------------- -

Field     Bits
-------   -----
PRE       64:33 (32) -- preamble
ST        32:31  (2) -- start of frame
OP        30:29  (2) -- operation code
(ADDR=00,WR=01,RD=11,RDINC=10)
PRTAD     28:26  (5) -- port address
DEVAD     25:19  (5) -- device address
TA        18:17  (2) -- bus turnaround phase & transfer acknowledge
ADDR/DATA 16:1  (16) -- address or data
IDLE         0   (1) -- end of transmission
                ----
                 65  -- transaction bit length
```

Fig. 7
(Prior Art)